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INTEGRATED CIRCUIT HAVING PHOTODIODE DEVICE
AND ASSOCIATED FABRICATION PROCESS

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority from prior French Patent Application No. 01-00420, filed January 12, 2001, the entire disclosure of which is herein incorporated by reference.

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BACKGROUND OF THE INVENTION

1.   Field of the Invention

The present invention relates to integrated circuits, and more specifically to integrated circuits that include photodiode-type semiconductor devices.

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2.   Description of Related Art

To produce a good photodiode is tricky. This is because it has to be sensitive to light and only the space charge region of the junction is capable of collecting the carriers generated by the light excitation, because of the electric field existing in this

20   region. Now, a photodiode is more sensitive the larger the space charge region. This means that the doping gradient at the junction is low. However, if the doping gradient is low, the capacitance of the junction is also low. Now, the role of a photodiode is to store, in this junction capacitor, the carriers generated in the space charge region.

The solution normally used consists in increasing the doping gradient of the

25   junction and the voltage applied to this junction. It is thus possible to obtain a wide space charge region combined with a high junction capacitance. Typically, a voltage of greater than 5 volts must be applied if the doping levels are high. However, current

submicron integrated circuits do not allow high voltages to be used since. In these technologies, the maximum supply voltage is less than 3.3 volts.

SUMMARY OF THE INVENTION

5   In view of these drawbacks, it is an object of the present invention to overcome the above-mentioned drawbacks and to decorrelate the doping gradient of the junction from the capacitance of the junction.

Another object of the present invention is to reduce the doping gradient at the junction so as to obtain a large extension of the space charge region even for low

10   applied voltages.

Yet another object of the present invention is to increase the capacitance associated with the junction, while neither increasing the footprint nor reducing the sensitivity of the photodiode for a given surface area.

A further object of the present invention is to produce a single-crystal substrate

15   that allows the subsequent formation of an epitaxial silicon layer free of crystal defects, in which layer a junction can be formed.

One embodiment of the present invention provides an integrated circuit that includes a substrate incorporating a semiconductor photodiode device having a p-n junction. The photodiode device includes at least one capacitive trench buried in the

20   substrate and connected in parallel with the junction. In a preferred embodiment, the substrate is formed from silicon, and the capacitive trench includes an internal doped silicon region partially enveloped by an insulating wall that laterally separates the internal region from the substrate.

Another embodiment of the present invention provides a method for

25   fabricating an integrated circuit including a substrate that incorporates a semiconductor photodiode device having a p-n junction. According to the method, there is produced an initial single-crystal substrate having locally a capacitive trench emerging at the surface of the initial substrate and forming a discontinuity in the crystal lattice. The initial substrate is recessed at the trench, and the crystal lattice is

amorphized around the periphery of the recess. A layer of amorphous material having the same chemical composition as the initial substrate is deposited, and a thermal annealing is performed in order to recrystallize the amorphous material so as to be continuous with the single-crystal lattice of the initial substrate. An upper substrate

5   layer is grown epitaxially. In one preferred method, the junction is formed by n^+-type surface codiffusion of arsenic and phosphorus.

Other objects, features, and advantages of the present invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating preferred

10   embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

15   Figures 1a to 1h illustrate a process for fabricating a photodiode device according to one embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail

20   hereinbelow with reference to the attached drawings.

One preferred embodiment of the present invention provides an integrated circuit that includes a substrate incorporating a semiconductor device of the photodiode type having a p-n junction. The device includes a capacitive trench buried in the substrate and connected in parallel with the junction.

25   Preferably, the junction has a low doping level or a low doping gradient, so that the length of the space charge region is greater than 1 micron even for low reverse voltages (for example, of less than 1 volt). For example, this can be achieved by a doping of less than 10^{15} at/cm^3 in the case of a sharp junction with low doping on only one side or else by a doping gradient of less than 10^{20} at/cm^3 in the case of a junction

with linear doping. Moreover, this parameter is decorrelated with the capacitance parameter. In this regard, the capacitance associated with the junction is increased by virtue of the presence of the buried capacitive trench, with neither an increase in surface area of the photodiode nor a loss of sensitivity.

5   According to one embodiment, the substrate is formed from silicon and the capacitive trench includes an internal doped silicon region partially enveloped by an insulating wall laterally separating the internal region from the substrate and surmounted by an upper doped silicon region, this upper region being in contact with the junction. Preferably, the substrate has a highly doped lower part with a p-type

10   conductivity, for example with a dopant concentration of greater than 10^{18} at/cm^3 (such as a dopant concentration equal to 10^{19} at/cm^3). The substrate also preferably has an upper part of p-type conductivity, less doped than the lower part. Also preferably, The internal region and the upper region of the capacitive trench have an n-type conductivity, and the region of the junction having the n-type conductivity

15   includes a lower region of n-type conductivity in contact with the upper region of the trench, and an upper region of n-type conductivity but more highly doped than the lower region. The use of a highly doped p-type substrate is not required, but it does allow the input resistances and the noise to be reduced.

        Processes for fabricating semiconductor components may destroy the crystal

20   continuity of the surface of part of the initial single-crystal semiconductor substrate. This is especially the case when a trench is produced. The semiconductor substrate has, at the position of the trench, a different material without any crystal structure. Consequently, the surface of that part of the substrate occupied by the trench cannot be used to produce semiconductor devices.

25   The present invention therefore also provides processes for fabricating an integrated circuit that includes a substrate incorporating a semiconductor device of the photodiode type having a p-n junction. According to the process of a preferred embodiment, an initial single-crystal substrate is produced, which has locally a capacitive trench emerging at the surface of the initial substrate and forming a

discontinuity in the crystal lattice. The initial substrate is recessed at the trench, and the crystal lattice is amorphized around the periphery of the recess. A layer of amorphous material having the same chemical composition as that of the initial substrate is next deposited on the structure, and then the structure is thermally

5   annealed in order to recrystallize the amorphous material so as to be continuous with the single-crystal lattice of the initial substrate. An upper substrate layer, in which the junction connected in parallel with the capacitive trench has been produced, is grown epitaxially.

According to one embodiment, prior or subsequent to the thermal annealing, a

10 surface planarization step is performed (for example, a chemical-mechanical polishing operation). Preferably, the junction is formed by n^+-type surface codiffusion of arsenic and phosphorus so as to reduce the doping gradient of the junction.

According to one embodiment, the amorphization step includes a localized ion implantation around the recess by a masking operation.

15 According to one embodiment, in the step of producing the initial substrate, a first layer of a first material and a second layer of a second material are deposited in succession on the initial substrate and then a trench is etched, and filled with a fill material. And in the step of recessing the initial substrate, the first layer and an upper portion of the trench fill material are selectively etched with respect to the second

20 layer so as to form lateral cavities and the recess at the crystal discontinuity, and the second layer is removed.

Preferably, in the step of producing the initial substrate, the filling of the trench includes lining the walls of the trench with oxide by thermal oxidation, depositing highly doped polycrystalline silicon in the trench so as to fill it, and etching

25 the polycrystalline silicon deposited previously so that the fill level of the trench is below the surface of the initial substrate.

One exemplary embodiment of a process for fabricating a photodiode device in accordance with the present invention will now be described in detail with reference to Figures 1a-1h. Figure 1a shows the starting substrate of the process, or

"initial substrate", which includes a trench in this embodiment. The initial substrate 1 has a p+-doped lower part (e.g., with a dopant concentration of 10^{19} at/cm^3), and a p-doped upper part grown epitaxially on the lower part (e.g., with a dopant concentration of 5×10^{14} at/cm^3).

5   The trench is formed, according to one embodiment of the present invention, by first depositing a silicon oxide layer 2 on the initial single-crystal silicon substrate 1. The thickness of this layer 2 may vary between 0.01 microns and 1 micron, and is preferably about 2000 Å. Next, a silicon nitride layer 3 is deposited on the oxide 2. The thickness of this layer 3 may also vary between 0.01 microns and 1 micron, and is
10   also preferably about 2000 Å. Next, the nitride 3, then the oxide 2, and finally the single-crystal silicon of the substrate 1 are conventionally etched with the aid of a photolithography operation in order to form the trench 4.

The trench 4 preferably has a depth of approximately 10 μm and a variable width, preferably less than 1 μm. Next, a controlled thermal oxidation is carried out
15   so as to deposit on the walls of the trench 4 a silicon oxide layer 8 having a thickness of between 40 and 1000 Å, preferably between 50 and 300 Å. This produces the device illustrated in Figure 1a.

Next, highly n+-doped polycrystalline silicon 9 is deposited on the wafer so as to fill the trench 4. The doping of the silicon is preferably carried out in situ. A
20   device as illustrated in Figure 1b is then obtained.

Next, the deposited polycrystalline silicon 9 is etched, at least so as to remove it from the surface of the wafer. Moreover, this etching is carried out until the level of the polycrystalline silicon in the trench 4 is below the surface of the initial substrate 1. Then, a controlled deoxidation is performed so as to form, under the silicon nitride
25   layer 3, two lateral cavities of given width in the oxide layer 2, as illustrated in Figure 1c. Some of the silicon oxide 8 in the trench 4 is also removed.

This deoxidation is preferably carried out by isotropic etching using hydrofluoric acid or by isotropic plasma etching using fluorine. The device illustrated in Figure 1c, in which the trench is lined with a silicon oxide layer 8 whose height is

less than the height of the doped polycrystalline silicon layer 9 in the trench 4, is then obtained. Two lateral cavities of given width appear below the silicon nitride layer 3 and in the silicon oxide layer 2.

Next, the silicon nitride mask 3 is conventionally removed. The exposed silicon is then amorphized. The silicon exposed at this stage of the process is the single-crystal silicon of the substrate 1 together with the emergent portion of doped polycrystalline silicon 9 in the trench 4. Thus, amorphous silicon regions 6 and 6a are created, as illustrated in Figure 1d. The localized simultaneous amorphization of the regions 6 and 6a is self-aligned with respect to the trench and is carried out conventionally by destroying the crystal lattice of the silicon and of the polycrystalline silicon 6a (for example, by the implantation of heavy particles such as ions). Within the context of the present invention, it is especially preferred to implant fluoride ions.

Next, an amorphous silicon layer 7 is deposited over the entire surface of the wafer so as to at least fill the lateral cavities and the recess above the trench 4. The deposited amorphous layer 7 therefore acts as a link between the regions 6 and 6a and as a means of filling in the surface. The amorphous silicon is preferably deposited conventionally at low temperature. For example, it is possible to use an LPCVD (low-pressure chemical vapor deposition) furnace, and inject silane at a sufficiently low temperature (for example, less than 600°C, and typically less than 400°C). The device illustrated in Figure 1d is then obtained. As shown, the device includes, in a trench 4 etched in the substrate 1, a polycrystalline silicon block 9 partially enveloped in a silicon oxide layer 8. The height of this block, which is less than that of the trench 4, is also less than the height of the silicon oxide envelope 8. This element is surmounted by an amorphous silicon region including the amorphized silicon regions 6 and 6a and the deposited amorphous silicon 7.

A thermal annealing operation is then carried out so as to restore the crystal structure of the amorphous silicon. The thermal annealing allows the amorphous silicon to recrystallize, by the epitaxial regrowth of the amorphous silicon 6 and 7 starting from the single-crystal silicon of the initial substrate 1. The restructuring of

the single-crystal silicon lattice results in the device of Figure 1e, in which the previous amorphous silicon layer now merges with the single-crystal silicon of the substrate 1.

It should be noted that, according to preferred embodiments of the present invention, the region 6 is spatially limited and the boundary between this region 6 and the substrate 1 is easily localized by ion implantation. This boundary is moreover a "soft" boundary. That is, the transition from the single-crystal Si state to the amorphous Si state is very gradual. These characteristics result in the region 6 being recrystallized very efficiently and without any defects, which is not easily achievable with a large area to be recrystallized.

In addition, the amorphization of the region 6a prevents crystal defects from "rising" into the single-crystal layer from the polycrystalline silicon.

Next, a chemical-mechanical polishing operation is carried out, stopping on the silicon oxide layer 2, in order to remove the recrystallized silicon layer on the surface of the wafer. The silicon oxide layer 2 is then conventionally removed. Next, in order to planarize the surface, the wafer is subjected to a final chemical-mechanical polishing operation.

After the planarizing of the surface of the substrate, a final single-crystal silicon substrate 10 is obtained, as illustrated in Figure 1f. The perfectly planar and uniform single-crystal surface of this substrate 10 allows defect-free epitaxial growth of single-crystal silicon. Preferably, the thickness of the substrate 10 above the trench is about 0.2 microns and is p-doped with a dopant concentration of about 5×10^{14} at/cm^3. Moreover, the substrate includes a buried capacitive trench TRC made of highly doped polycrystalline silicon 90 partially enveloped by a silicon oxide wall 8 that separates it laterally from the substrate 1. Above this buried capacitive trench and in the substrate 1, there remains a doped region 1a, of the same conductivity as the polycrystalline silicon 90. This region corresponds to the amorphized polycrystalline silicon region 6a and to the silicon portion 7 doped by the diffusion of dopants during the annealing.

The localized destruction of the crystal lattice that is performed according to the present invention is particularly advantageous in the case of capacitive trenches, as it allows the polycrystalline silicon 90 (the entire capacitor) to be buried by controlled etching of the sidewall oxide 8, without it being necessary to provide an additional

5   oxide.

As shown in Figure 1g, the process is continued by epitaxial growth on the surface of the substrate 10 of an upper substrate layer 12, formed from p-doped silicon and preferably having a thickness of approximately two microns. It is in this layer 12 that the junction will be formed.

10   More specifically, as illustrated in Figure 1h, the substrate SB, which is formed from the substrate 10 and the layer 12, incorporates the capacitive trench TRC and the junction. The upper region 1a of the trench comes into direct contact with the n-doped lower region LR of the p-n junction. This lower region LR is obtained, for example, by phosphorus implantation with a concentration of approximately

15   3×10^{15} at/cm^2 with an energy of approximately 100 keV. The n-type region of the junction also preferably has an n-type upper region UR more highly doped than the lower region LR. For example, in one embodiment this region UR is formed by arsenic implantation with a concentration of approximately 5×10^{15} at/cm^2 with an energy of approximately 60 keV. The codiffusion of the dopants is achieved by a

20   thermal annealing operation, for example at a temperature of 1000°C for 20 minutes.

The right side of Figure 1h shows the equivalent circuit diagram of the photodiode, showing that the capacitive trench is connected in parallel with the p-n junction.

The carriers generated are collected and handled in a known conventional

25   manner, for example using a MOS transistor or else a charge-coupled device (CCD).

It should also be noted that should there be matricing of this photodiode, the presence of the buried trench does not create a light-insensitive region.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those

skilled in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the present invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive

5   concept described herein. Furthermore, an embodiment of the present invention may not include all of the features described above. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.